Claim 4 should be replac d with:

4. (Amended) The flip-flop of claim 3, further comprising a first clock terminal connected to the first-mentioned control terminal and a second clock terminal connected to the second control terminal.

Claim 9 should be replaced with:

9. (Amended) The flip-flop of claim 8, wherein the control and second control terminals are adapted to receive complementary clock signals.

Claim 10 should be replaced with:

10. (Amended) A flip-flop comprising a differential input stage having differential first and second input terminals, differential third and fourth input terminals, a first transistor, and complementary first and second output terminals, wherein the first transistor has a first control terminal connected to the first input terminal and a current handling terminal directly connected to VSS.

Claim 11 should be replaced with:

11. (Amended) The flip-flop of claim 10, wherein the input stage further comprises a first leg including the first transistor and a second transistor connected in parallel, the second transistor having a second control terminal connected to the third input terminal.

Claim 17 should be replaced with:

17. (Amended) A counter circuit comprising:

a. a first flip-flop having:

i. a differential output stage having differential first and second input terminals and complementary first and second output terminals; and

ii. a first transistor having a first current-handling terminal connected to the first output

terminal, a second current-handling terminal connected to the second output terminal, and a first control terminal; and

iii. a cross coupled circuit having a cross coupled transistor directly connected to a power supply voltage, wherein a gate of the cross coupled transistor is connected to the second output terminal; and

b. a second flip-flop having:

i. a differential input stage having differential third and fourth input terminals connected to the respective first and second output terminals of the first flip-flop, a second transistor, and complementary third and fourth output terminals, the second transistor having a gate connected to the third input terminal and a current handling terminal directly connected to VSS; and

ii. a third transistor having a third current-handling terminal connected to the third output terminal, a fourth current-handling terminal connected to the fourth output terminal, and a second control terminal.